WHAT IS CLAIMED IS

1. A radiofrequency signal receiver including means for receiving and shaping said radiofrequency signals into intermediate signals, a correlation stage which includes several correlation channels for receiving the intermediate signals, microprocessor means connected to said correlation stage for the transfer of control and/or data signals, wherein it includes channel selection means connected to all the channels of the correlation stage and to the microprocessor means, said selection means allowing the channel with the highest priority among the operating channel or channels which have each transmitted an interruption signal for a data transfer from the selected channel to the microprocessor means, to be placed first in a virtual channel, in accordance with a defined order of priority for all the channels.

2. A receiver according to claim 1, wherein the selection means are a priority decoder wherein each correlation channel is represented by its identification number so as to define the order of priority as a function of this identification number, the channel having the highest priority being that whose determined identification number is the highest or the lowest among the operating channel or channels having each transmitted an interruption signal for a data transfer from the selected channel to the microprocessor means.

3. A receiver according to one of claims 1 and 2, wherein, after reading the data from the selected channel placed in the virtual channel, the microprocessor means transmit a read confirmation signal to said channel in order to cancel the interruption caused by this channel and to select the next channel with the highest priority which has transmitted an interruption signal.

4. A receiver according to claim 2, wherein the priority decoder includes a number of multiplexers placed one after the other corresponding to the number of channels to be controlled, for example 12 channels, the output of each multiplexer being connected to an input of a following multiplexer except for the output of the last multiplexer intended to select the channel with the highest priority, each multiplexer receiving at another input the identification number of a respective channel in a defined order, an interruption signal from each channel instructing the respective multiplexer to transmit at its output the identification number of the channel when an interruption signal from said channel is applied to said respective multiplexer.

5. A receiver according to claim 1, wherein each correlation channel includes a correlator receiving the intermediate signals, and a controller for

implementing an algorithm for processing the digital signals in all the synchronisation tasks during the search and tracking of a determined satellite.

6. A receiver according to claim 2, wherein the correlation stage, the microprocessor means and the priority decoder are made on a same semiconductor substrate, for example made of silicon.